What Is Claimed Is:

1. A digital adjustable chip oscillator, comprising:

a voltage control oscillator generating an oscillation signal, receiving a control voltage to adjust the frequency of the oscillation signal, and receiving an operating voltage to stabilize the frequency of the oscillation signal;

a reference voltage circuit generating a reference voltage;

a voltage regulation circuit receiving the reference voltage and generating the operating voltage;

a digital tuning circuit receiving a digital code to adjust the control voltage and receiving the operating voltage to stabilize the control voltage;

a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the frequency of the oscillation signal lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal;

a programmable counter receiving a clock signal to trigger the counting and generating the digital code;

a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high

voltage comparison signal and directing the programmable counter to stop counting and hold the digital code; and

a programmable memory receiving the enable signal to record the digital code.

2. The digital adjustable chip oscillator as claimed in claim 1, wherein the voltage control oscillator is a relaxation oscillator.

3. The digital adjustable chip oscillator as claimed in claim 1, wherein the reference voltage circuit is a bandgap reference voltage circuit.

4. The digital adjustable chip oscillator as claimed in claim 1, wherein the voltage regulation circuit comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting a bias voltage;

a transistor receiving the bias voltage, outputting a current, and outputting the operating voltage; and

a loop circuit receiving the current and outputting the loop voltage.

5. The digital adjustable chip oscillator as claimed in claim 1, wherein the digital tuning circuit comprises:

a plurality of current mirrors receiving a bias voltage to generate a plurality of bias currents corresponding to the bit of the digital code and

receiving the operating voltage to stabilize the plurality of bias currents;

a transistor receiving the plurality of bias currents to generate the control voltage; and

a plurality of switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of current mirrors.

6. The digital adjustable chip oscillator as claimed in claim 5, further comprising a prescaler receiving the oscillation signal and generating a period dividing signal according to a period dividing code.

7. The digital adjustable chip oscillator as claimed in claim 6, wherein the digital tuning circuit further comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting the bias voltage;

a transistor receiving the bias voltage, outputting a reference current, and proportioning the bias current of the plurality of current mirrors to the reference current wherein the bias voltage is coupled to the plurality of current mirrors; and

a loop circuit receiving the reference current and outputting the loop voltage.

8. The digital adjustable chip oscillator as claimed in claim 1, wherein the digital tuning circuit further comprises:

a plurality of charge current mirrors receiving a bias voltage to generate a plurality of bias currents corresponding to the bit of the digital code and receiving the operating voltage to stabilize the plurality of bias currents;

a plurality of discharge current mirrors receiving the bias current to generate a plurality of bias currents corresponding to the bit of the digital code;

a transistor receiving the plurality of bias currents to generate the control voltage;

a plurality of first switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of charge current mirrors; and

a plurality of second switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of charge current mirrors.

9. The digital adjustable chip oscillator as claimed in claim 1, wherein the programmable memory is a programmable fuse.

10. The digital adjustable chip oscillator as claimed in claim 1, wherein the programmable memory is a programmable gate writer.

11. The digital adjustable chip oscillator as claimed in claim 1, wherein the frequency detector comprises:

a first phase frequency detector receiving the first reference signal, receiving the oscillation signal, and generating a first detection signal;

a first low-pass filter receiving the first detection signal and outputting the dc component of the first detection signal;

a first comparator receiving the dc component of the first detection signal and generating a first comparison signal wherein when the first reference frequency lies above the oscillation frequency, the first comparison signal is high-level, otherwise the first comparison signal is low-level;

a second phase frequency detector receiving the second reference signal, receiving the oscillation signal, and generating a second detection signal;

a second low-pass filter receiving the second detection signal and outputting the dc component of the second detection signal;

a second comparator receiving the dc component of the second detection signal and generating a second comparison signal wherein when the second reference frequency lies above the oscillation frequency, the second comparison signal is high-level, otherwise the second comparison signal is low-level; and

an exclusive gate receiving the first comparison signal, receiving the second comparison signal, and generating the comparison signal.

12. The digital adjustable chip oscillator as claimed in claim 11, wherein the first low-pass filter and the second low-pass filter are both switch capacitance filters.

13. The digital adjustable chip oscillator as claimed in claim 1, wherein the voltage control oscillator and the digital tuning circuit both have power save mode.

14. A digital adjustable chip oscillator, comprising:

a voltage control oscillator generating an oscillation signal, receiving a control voltage to adjust the frequency of the oscillation signal, and receiving an operating voltage to stabilize the frequency of the oscillation signal;

a reference voltage circuit generating a reference voltage;

a voltage regulation circuit receiving the reference voltage and generating the operating voltage; and

a digital tuning circuit receiving a digital code to adjust the control voltage and receiving the operating voltage to stabilize the control voltage.

15. The digital adjustable chip oscillator as claimed in claim 14, wherein the voltage control oscillator is a relaxation oscillator.

16. The digital adjustable chip oscillator as claimed in claim 14, wherein the reference voltage circuit is a bandgap reference voltage circuit.

17. The digital adjustable chip oscillator as claimed in claim 5, further comprising a prescaler receiving the oscillation signal and generating a period dividing signal according to a period dividing code.

18. The digital adjustable chip oscillator as claimed in claim 14, wherein the voltage regulation circuit comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting a bias voltage;

a transistor receiving the bias voltage, outputting a current, and outputting the operating voltage; and

a loop circuit receiving the current and outputting the loop voltage.

19. The digital adjustable chip oscillator as claimed in claim 14, wherein the digital tuning circuit comprises:

a plurality of current mirrors receiving a bias voltage to generate a plurality of bias currents corresponding to the bit of the digital code and receiving the operating voltage to stabilize the plurality of bias currents;

a transistor receiving the plurality of bias currents to generate the control voltage; and

a plurality of switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of current mirrors.

20. The digital adjustable chip oscillator as claimed in claim 14, wherein the digital tuning circuit further comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting the bias voltage;

a transistor receiving the bias voltage, outputting a reference current, and proportioning the bias current of the plurality of current mirrors to the reference current wherein the bias voltage is coupled to the plurality of current mirrors; and

a loop circuit receiving the reference current and outputting the loop voltage.

21. The digital adjustable chip oscillator as claimed in claim 14, wherein the digital tuning circuit further comprises:

a plurality of charge current mirrors receiving a bias voltage to generate a plurality of bias currents corresponding to the bit of the digital code and receiving the operating voltage to stabilize the plurality of bias currents;

a plurality of discharge current mirrors receiving the bias current to generate a plurality of bias currents corresponding to the bit of the digital code;

a transistor receiving the plurality of bias currents to generate the control voltage;

a plurality of first switches coupled to the plurality of current mirrors and the transistor and

receiving the digital code to select the plurality of charge current mirrors; and

a plurality of second switches coupled to the plurality of current mirrors and the transistor and receiving the digital code to select the plurality of charge current mirrors.

22. The digital adjustable chip oscillator as claimed in claim 14, wherein it further comprises:

a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the oscillation frequency lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal;

a programmable counter receiving a clock signal to trigger the counting and generating the digital code;

a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the digital code; and

a programmable memory receiving the enable signal to record the digital code.

23. The digital adjustable chip oscillator as claimed in claim 22, wherein the programmable memory comprises:

a plurality of decoders; and

a plurality of poly-silicon fuses.

24. The digital adjustable chip oscillator as claimed in claim 22, wherein the programmable memory is a programmable gate writer.

25. The digital adjustable chip oscillator as claimed in claim 22, wherein the frequency detector comprises:

a first phase frequency detector receiving the first reference signal, receiving the oscillation signal, and generating a first detection signal;

a first low-pass filter receiving the first detection signal and outputting the dc component of the first detection signal;

a first comparator receiving the dc component of the first detection signal and generating a first comparison signal wherein when the first reference frequency lies above the oscillation frequency, the first comparison signal is high-level, otherwise the first comparison signal is low-level;

a second phase frequency detector receiving the second reference signal, receiving the oscillation signal, and generating a second detection signal;

a second low-pass filter receiving the second detection signal and outputting the dc component of the second detection signal;

a second comparator receiving the dc component of the second detection signal and generating a second comparison signal wherein when the second reference frequency lies above the oscillation frequency, the second comparison signal is high-level, otherwise the second comparison signal is low-level; and

an exclusive gate receiving the first comparison signal, receiving the second comparison signal, and generating the comparison signal.

26. The digital adjustable chip oscillator as claimed in claim 25, wherein the first low-pass filter and the second low-pass filter are both switch capacitance filters.

27. A digital adjustable chip oscillator, comprising:

a voltage control oscillator generating an oscillation signal and receiving a control voltage to control the frequency of the oscillation signal;

a frequency-to-voltage converter receiving the oscillation signal and generating a loop voltage based on an operating voltage and a first voltage;

an active comparison filter receiving the loop voltage, receiving a second voltage, and generating the control voltage; and

a first programmable controller receiving a first digital code, receiving the operating voltage, and generating the second voltage.

28. The digital adjustable chip oscillator as claimed in claim 27, further comprising a reference voltage circuit

generating the reference voltage wherein the reference voltage circuit is a bandgap reference voltage circuit.

29. The digital adjustable chip oscillator as claimed in claim 27, further comprising a voltage regulation circuit receiving the reference voltage and generating the operating voltage.

30. The digital adjustable chip oscillator as claimed in claim 27, wherein the voltage regulation circuit comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting a bias voltage;

a transistor receiving the bias voltage, outputting a current, and outputting the operating voltage; and

a loop circuit receiving the current and outputting the loop voltage.

31. The digital adjustable chip oscillator as claimed in claim 27, further comprising a prescaler receiving the oscillation signal, generating a period dividing signal based on a period dividing code, and outputting the a period dividing signal to the frequency-to-voltage converter.

32. The digital adjustable chip oscillator as claimed in claim 31, further comprising a delay circuit receiving the period dividing signal, generating a delay signal, and outputting the delay signal to the frequency-to-voltage converter wherein the operating period of the delay signal

satisfies the requirement of the frequency-to-voltage converter.

33. The digital adjustable chip oscillator as claimed in claim 27, wherein the first programmable controller comprises:

a resistor serial having a plurality of resistors, receiving the operating voltage, and generating the second voltage from the output end;

a plurality of switches coupled to the corresponding connection point of the plurality of resistors and the output end of the programmable controller; and

a decoder receiving the first digital code to select the corresponding switch.

34. The digital adjustable chip oscillator as claimed in claim 27, wherein the frequency-to-voltage converter comprises:

a first capacitor;

a second capacitor;

an amplifier having an input end, a reversed-phase input end, and an output end wherein the input end of the amplifiers is coupled to the first voltage;

a third capacitor coupled to the reversed-phase input end of the amplifier and the output end of the amplifier;

a first switch coupled to the input end of the frequency-to-voltage converter and the reversed-phase input end of the reversed-phase amplifier wherein the control end of the first switch

receives a signal having the phase opposite to the phase of the oscillation signal;

a second switch coupled to the reversed-phase input end of the reversed-phase amplifier and the second capacitor wherein the control end of the second switch receives the output signal of the voltage control oscillator;

a voltage control current source coupled to the second capacitor wherein the input end of the voltage control current source receives the output end voltage of the reversed-phase amplifier and the output end of the voltage control current source generates a balance current; and

a current-to-voltage converter circuit of which the input end is coupled to the input end of the voltage control current source and the output end is coupled to a resistor wherein the current of the resistor is proportional to the balance current.

35. The digital adjustable chip oscillator as claimed in claim 27, wherein the digital adjustable chip oscillator further comprises a second programmable controller receiving a second digital code to select the input current of the resistor in the current-to-voltage converter circuit.

36. The digital adjustable chip oscillator as claimed in claim 35, wherein the second programmable controller comprises:

a plurality of current mirrors wherein each bias point of the current mirrors is coupled to the input end

of the voltage control current source, the current generated by the output end of the voltage control current source is a multiple of the balance current, and the multiplication factor corresponds to the bit of the digital code; and

a plurality of switches coupled to the output end of the correspondent above-mentioned plurality of current mirrors and the output end of the frequency-to-voltage converter and receiving the digital code to select the plurality of current mirrors.

37. The digital adjustable chip oscillator as claimed in claim 27, wherein the active comparison filter is a proportional integral filter.

38. The digital adjustable chip oscillator as claimed in claim 27, wherein the active comparison filter comprises:

a differential amplifier having an input end, a reversed-phase input end, and an output end wherein the input end of the differential amplifier receives the second voltage

a first resistor of which one end receives the loop voltage and the other end is coupled to the reversed-phase input end of the differential amplifier;

a first capacitor coupled to the reversed-phase input end of the differential amplifier and the output end of the differential amplifier;

a second resistor of which one end is coupled to the reversed-phase input end of the differential amplifier; and

a second capacitor coupled to the other end of the second resistor and the output end of the differential amplifier.

39. The digital adjustable chip oscillator as claimed in claim 27, further comprising a voltage limiter receiving the control voltage output by the active comparison filter and limiting the control voltage in the input range of the voltage control oscillator.

40. The digital adjustable chip oscillator as claimed in claim 27, wherein the voltage control oscillator comprises a plurality of differential delay units connected in the form of a ring wherein each of the differential delay unit has a control end to receive the control voltage and adjust the delay time, and has a pair of differential inputs and a pair of differential outputs.

41. The digital adjustable chip oscillator as claimed in claim 40, wherein the voltage control oscillator further comprises a differential single-end converter having a pair of differential inputs and a single-end output end wherein the pair of differential inputs of the differential single-end converter is coupled to an output pair of the differential delay unit.

42. The digital adjustable chip oscillator as claimed in claim 40, wherein the voltage control oscillator further

comprises an output buffer of which the input end is coupled to the single-end output end of the differential single-end converter, and the signal of the output end is a full amplitude signal.

43. The digital adjustable chip oscillator as claimed in claim 27, further comprising:

a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the oscillation frequency lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal;

a programmable counter receiving a clock signal to trigger the counting and generating the first digital code;

a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the digital code; and

a programmable memory receiving the enable signal to record the digital code.

44. The digital adjustable chip oscillator as claimed in claim 43, wherein the programmable memory is a programmable fuse.

45. The digital adjustable chip oscillator as claimed in claim 1, wherein the programmable memory is a programmable gate writer.

46. The digital adjustable chip oscillator as claimed in claim 27, further comprising:

a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the oscillation frequency lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal;

a programmable counter receiving a clock signal to trigger the counting and generating the first digital code and the second digital code;

a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the first digital code and the second digital code; and

a programmable memory receiving the enable signal to record the first digital code and the second digital code.

47. The digital adjustable chip oscillator as claimed in claim 43, wherein the frequency detector comprises:

a first phase frequency detector receiving the first reference signal, receiving the oscillation signal, and generating a first detection signal;

a first low-pass filter receiving the first detection signal and outputting the dc component of the first detection signal;

a first comparator receiving the dc component of the first detection signal and generating a first comparison signal wherein when the first reference frequency lies above the oscillation frequency, the first comparison signal is high-level, otherwise the first comparison signal is low-level;

a second phase frequency detector receiving the second reference signal, receiving the oscillation signal, and generating a second detection signal;

a second low-pass filter receiving the second detection signal and outputting the dc component of the second detection signal;

a second comparator receiving the dc component of the second detection signal and generating a second comparison signal wherein when the second reference frequency lies above the oscillation frequency, the second comparison signal is high-level, otherwise the second comparison signal is low-level; and

an exclusive gate receiving the first comparison signal, receiving the second comparison signal, and generating the comparison signal.

48. The digital adjustable chip oscillator as claimed in claim 47, wherein the first low-pass filter and the second low-pass filter are both switch capacitance filters.

49. A digital adjustable chip oscillator, comprising:

a voltage control oscillator generating an oscillation signal and receiving a control voltage to control the frequency of the oscillation signal;

a frequency-to-voltage converter receiving the oscillation signal and generating a loop voltage based on an operating voltage and a first voltage;

an active comparison filter receiving the loop voltage, receiving a second voltage, and generating the control voltage; and

a first programmable controller receiving a first digital code, receiving the operating voltage, and generating the second voltage.

a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the frequency of the oscillation signal lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal;

a programmable counter receiving a clock signal to trigger the counting and generating the first digital code;

a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the first digital code; and

a programmable memory receiving the enable signal to record the first digital code.

50. The digital adjustable chip oscillator as claimed in claim 49, further comprising a reference voltage circuit generating the reference voltage wherein the reference voltage circuit is a bandgap reference voltage circuit.

51. The digital adjustable chip oscillator as claimed in claim 49, further comprising a voltage regulation circuit receiving the reference voltage and generating the operating voltage.

52. The digital adjustable chip oscillator as claimed in claim 49, wherein the voltage regulation circuit comprises:

an operational transconductance amplifier receiving the reference voltage, receiving a loop voltage, and outputting a bias voltage;

a transistor receiving the bias voltage, outputting a current, and outputting the operating voltage; and

a loop circuit receiving the current and outputting the loop voltage.

53. The digital adjustable chip oscillator as claimed in claim 49, wherein the first programmable controller comprises:

a resistor serial having a plurality of resistors, receiving the operating voltage, and generating the second voltage from the output end;

a plurality of switches coupled to the corresponding connection point of the plurality of resistors and the output end of the programmable controller; and

a decoder receiving the first digital code to select the corresponding switch.

54. The digital adjustable chip oscillator as claimed in claim 49, wherein the frequency-to-voltage converter comprises:

a first capacitor;

a second capacitor;

an amplifier having an input end, a reversed-phase input end, and an output end wherein the input end of the amplifiers is coupled to the first voltage;

a third capacitor coupled to the reversed-phase input end of the amplifier and the output end of the amplifier;

a first switch coupled to the input end of the frequency-to-voltage converter and the reversed-phase input end of the reversed-phase amplifier wherein the control end of the first switch

receives a signal having a phase opposite to the phase of the oscillation signal;

a second switch coupled to the reversed-phase input end of the reversed-phase amplifier and the second capacitor wherein the control end of the second switch receives the output signal of the voltage control oscillator;

a voltage control current source coupled to the second capacitor wherein the input end of the voltage control current source receives the output end voltage of the reversed-phase amplifier and the output end of the voltage control current source generates a balance current; and

a current-to-voltage converter circuit of which the input end is coupled to the input end of the voltage control current source and the output end is coupled to a resistor wherein the current of the resistor is proportional to the balance current.

55. The digital adjustable chip oscillator as claimed in claim 49, further comprising a prescaler receiving the oscillation signal, generating a period dividing signal based on a period dividing code, and outputting the period dividing signal to the frequency-to-voltage converter.

56. The digital adjustable chip oscillator as claimed in claim 55, further comprising a delay circuit receiving the period dividing signal, generating a delay signal, and outputting the delay signal to the frequency-to-voltage converter wherein the operating period of the delay signal

satisfies the requirement of the frequency-to-voltage converter.

57. The digital adjustable chip oscillator as claimed in claim 49, further comprising a second programmable controller receiving a second digital code to select the input current of the resistor in the current-to-voltage converter circuit.

58. The digital adjustable chip oscillator as claimed in claim 57, wherein the second programmable controller comprises:

a plurality of current mirrors wherein each bias point of the current mirrors is coupled to the input end of the voltage control current source, the current generated by the output end of the voltage control current source is a multiple of the balance current, and the multiplication factor corresponds to the bit of the digital code; and

a plurality of switches coupled to the output end of the correspondent above-mentioned plurality of current mirrors and the output end of the frequency-to-voltage converter and receiving the digital code to select the plurality of current mirrors.

59. The digital adjustable chip oscillator as claimed in claim 49, wherein the active comparison filter is a proportional integral filter.

60. The digital adjustable chip oscillator as claimed in claim 49, wherein the active comparison filter comprises:

a differential amplifier having an input end, a reversed-phase input end, and an output end wherein the input end of the differential amplifier receives the second voltage

a first resistor of which one end receives the loop voltage and the other end is coupled to the reversed-phase input end of the differential amplifier;

a first capacitor coupled to the reversed-phase input end of the differential amplifier and the output end of the differential amplifier;

a second resistor of which one end is coupled to the reversed-phase input end of the differential amplifier; and

a second capacitor coupled to the other end of the second resistor and the output end of the differential amplifier.

61. The digital adjustable chip oscillator as claimed in claim 49, further comprising a voltage limiter receiving the control voltage output by the active comparison filter and limiting the control voltage in the input range of the voltage control oscillator.

62. The digital adjustable chip oscillator as claimed in claim 49, wherein the voltage control oscillator comprises a plurality of differential delay units connected in the form of a ring wherein each of the differential delay

unit has a control end to receive the control voltage and adjust the delay time, and has a pair of differential inputs and a pair of differential outputs.

63. The digital adjustable chip oscillator as claimed in claim 62, wherein the voltage control oscillator further comprises a differential single-end converter having a pair of differential inputs and a single-end output end wherein the pair of differential inputs of the differential single-end converter is coupled to an output pair of the differential delay unit.

64. The digital adjustable chip oscillator as claimed in claim 63, wherein the voltage control oscillator further comprises an output buffer of which the input end is coupled to the single-end output end of the differential single-end converter, and the signal of the output end is a full amplitude signal.

65. The digital adjustable chip oscillator as claimed in claim 49, wherein the programmable memory is a programmable fuse.

66. The digital adjustable chip oscillator as claimed in claim 49, wherein the programmable memory is a programmable gate writer.

67. The digital adjustable chip oscillator as claimed in claim 49, wherein the frequency detector comprises:

a first phase frequency detector receiving the first reference signal, receiving the oscillation signal, and generating a first detection signal;

a first low-pass filter receiving the first detection signal and outputting the dc component of the first detection signal;

a first comparator receiving the dc component of the first detection signal and generating a first comparison signal wherein when the first reference frequency lies above the oscillation frequency, the first comparison signal is high-level, otherwise the first comparison signal is low-level;

a second phase frequency detector receiving the second reference signal, receiving the oscillation signal, and generating a second detection signal;

a second low-pass filter receiving the second detection signal and outputting the dc component of the second detection signal;

a second comparator receiving the dc component of the second detection signal and generating a second comparison signal wherein when the second reference frequency lies above the oscillation frequency, the second comparison signal is high-level, otherwise the second comparison signal is low-level; and

an exclusive gate receiving the first comparison signal, receiving the second comparison signal, and generating the comparison signal.

68. The digital adjustable chip oscillator as claimed in claim 67, wherein the first low-pass filter and the second low-pass filter are both switch capacitance filters.